

## **SELF-REFRESH APPARATUS AND METHOD**

### **BACKGROUND OF THE INVENTION**

#### **1. Field of the Invention**

5        The present invention relates to a self-refresh apparatus and method for correctinh self-refresh rate error which may be generated when a partial array self-refresh (hereinafter, referred to as "PASR") operation is performed on a half of bank or a quarter of bank.

10

#### **2. Description of the Background Art**

      A DRAM is used as a main memory device in most computer systems, whose cell requires a refresh operation to prevent loss of data.

15

      A conventional semiconductor memory device performs a refresh operation on all cell arrays regardless of data storage in each cell, because an additional memory means for memorizing whether data are stored in each cell is required in the memory device.

20

      As a result, a PASR operation is performed in order to solve the above-described problem.

      The PASR operation may reduce power consumption because it is performed on a cell array having data during the same cycle.

For example, if a refresh operation is performed on only a half of a bank during a refresh rate, power consumption is reduced in half.

Fig. 1 is a diagram illustrating a self-refresh operation performed on cell arrays of a bank in a conventional memory 10 comprising four banks.

The memory cell arrays of a bank <2> are divided into two "HALF OF BANK"s(HOB) 15 and 16. Wordlines 11 and 12 are first and last wordlines of the "HALF OF BANK" 15. Wordlines 13 and 14 are first and last wordlines of the "HALF OF BANK" 16.

Fig. 2 is a timing diagram illustrating a self-refresh operation performed on "ALL BANK" for explaining a refresh rate. Fig. 3 is a timing diagram illustrating a self-refresh operation performed on "HALF of BANK" for explaining the refresh rate error.

When a refresh operation is performed on the bank <2>, an internal counter counts from wordline 11 to wordline 14. Here, a refresh rate is supposed to be 64msec.

When an auto-refresh or self-refresh command (ALL BANK PASR) is performed on the whole bank <2>, the refresh operation time on each "HALF OF BANK" 15 and 16 is 32m/sec. The refresh operation time on the whole bank <2> is 64m/sec. That is, all wordlines 11~14 should be consecutively

activated in order to refresh all cells on the bank <2>.

Here, it takes about 64m/sec to re-activate the first wordline 11.

When the PASR operation is performed on a "HALF OF BANK", the wordlines 11~12 are consecutively activated for 64msec.

According to a method of performing the PASR operation on the "half of bank" for 64msec, the pulse interval of the refresh requiring signal is extended twice as much, and only internal addresses of cell arrays storing data are counted. Further, when a PASR operation is performed on a "QUARTER OF BANK" for 64msec, the pulse interval of the refresh requiring signal is extended four times as much, and only internal address of cell arrays storing data are counted.

However, when the above-described self-refresh operation is performed on the "HALF OF BANK", a self-refresh command on the "HALF OF BANK" is set as an EMRS (Extended Mode Register Set) code, and then the self-refresh operation is performed on the wordlines 11~12, consecutively. After the self-refresh operation is performed on the wordline 12, the self-refresh operation is finished by an external command. Here, the self-refresh time performed on the wordlines 11~12 is 64msec.

As shown in Figs. 2 and 3, the section "B" of Fig. 3 is twice longer than the section "A" of Fig. 2.

After the self-refresh operation is finished, an auto-refresh is performed pursuant to an auto-refresh 5 command during the normal operation. Here, the internal address counter starts to count the wordline 13 in response to the auto-refresh command because the self-refresh operation is finished at the wordline 12.

That is, if the self-refresh operation is not 10 finished, the internal address counter starts to recount the wordline 11. However, since the self-refresh operation is finished, the internal address counter starts to count the wordline 13 by a pulse interval "A" of Fig. 2.

It takes 32msec to perform the auto-refresh operation 15 consecutively from the wordline 13 to the wordline 14. As a result, it takes 96msec to re-perform a refresh operation on the wordline 11 as shown in Fig. 3.

The refresh operation is performed on the wordline 11 after 96msec although the refresh operation should be 20 performed on each wordline per about 64msec in a memory having a refresh rate of 64msec, which may cause loss of data.

## **SUMMARY OF THE INVENTION**

Accordingly, it is an object of the present invention to provide a self-refresh apparatus which prevents refresh rate error by counting internal address in a predetermined cycle corresponding to a refresh rate regardless of types of PASR in a PASR mode.

In an embodiment, there is provided a self-refresh apparatus comprising an internal address counter, a refresh controller and a row address strobe generator.

10 The refresh controller outputs a signal as an internal operation signal for counting internal address in response to a refresh command signal. Here, the signal has a predetermined cycle corresponding to a refresh rate

The internal address counter counts internal address 15 in response to the internal operation signal.

When a PASR command signal on a bank is applied, the refresh controller selectively outputs the signal having a predetermined cycle depending on counting values of the internal address. Here, the signal is used as a refresh 20 operation signal for activating the bank. The row address strobe generator selectively activates the bank in response to the refresh operation signal.

In an embodiment, there is provided a self-refresh method wherein when a PASR operation is performed on a bank,

internal address on the bank is continuously counted in a predetermined cycle corresponding to a refresh rate regardless of types of the PASR. However, the corresponding bank is activated only while the internal 5 address is counted to a predetermined address depending on types of the partial array self-refresh.

The self-refresh method for performing a PASR operation on a semiconductor memory comprises: the first step of activating a refresh operation signal for 10 activating a bank and an internal operation signal for counting internal address, when a PASR command on a bank is applied; the second step of checking state change of a specific bit of the counted internal address depending on states of the PASR; and the third step of continuously 15 activating the internal operation signal in a predetermined cycle regardless of state change of the specific bit, and of inactivating the refresh operation signal when the state of the specific bit is changed.

## 20 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram illustrating a structure of general memory bank.

Fig. 2 is a diagram illustrating a refresh rate.

Fig. 3 is a diagram illustrating error of the refresh

rate.

Fig. 4 is a diagram illustrating an EMRS code according to an embodiment of the present invention.

Fig. 5 is a timing diagram illustrating a self-refresh entry and exit mode according to an embodiment of the present invention.

Fig. 6 is a structural diagram illustrating a self-refresh apparatus according to an embodiment of the present invention.

Fig. 7 is a diagram illustrating the relationship between a self-refresh signal and a self-refresh request signal which are activated in response to external commands.

Fig. 8 is a detailed structural diagram illustrating a PASR decoder of Fig. 6.

Fig. 9 is a detailed circuit diagram illustrating an EMRS decoder of Fig. 8.

Fig. 10 is a detailed circuit diagram illustrating an EMRS address latch of Fig. 8.

Fig. 11 is a detailed circuit diagram illustrating a PASR controller of Fig. 8.

Fig. 12 is a detailed circuit diagram illustrating a refresh controller of Fig. 6.

Fig. 13 is a detailed circuit diagram illustrating a RAS generator <0> of Fig. 6.

Fig. 14 is a detailed circuit diagram illustrating a RAS generator <1> ~ <3> of Fig. 6.

Fig. 15 is a timing diagram illustrating the operation of control signals for controlling the RAS generator of Fig. 14.

#### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

The present invention will be described in detail with reference to the accompanying drawings.

Fig. 4 is a diagram illustrating an EMRS code where a refresh type of a refresh apparatus according to an embodiment of the present invention is applied.

Addresses A0~A2 of the EMRS code are used for PCSR setup. As a result, when an EMRS command is inputted externally, the refresh apparatus performs a corresponding self-refresh operation depending on EMRS codes as shown in Fig. 4.

When the addresses A0~A2 are all 0, a self-refresh operation is performed on the whole cell array by selecting "ALL BANKS".

When only the address A0 is 1, a self-refresh operation is performed on a half of the whole cell array by selecting a "HALF ARRAY". As shown in Fig. 1, in a DRAM having a four-bank structure, the self-refresh operation is

performed on two banks. Here, a bank selecting address BA1 becomes 0.

When only the address A1 is 1, a self-refresh operation is performed on a quarter of the whole cell array 5 by selecting a "QUARTER ARRAY". As shown in Fig. 1, in a DRAM having a four-bank structure, the self-refresh operation is performed on a bank. Here, bank selecting addresses BA0 and BA1 become both 0.

When only the address A1 is 0, a self-refresh 10 operation is performed on a half cell array of a bank by selecting a "HALF of BANK". For example, a self-refresh operation is performed on cell arrays corresponding to the "HALF of BANK" 15 of the bank <2> in Fig. 1. Here, one of the bank selecting addresses BA0 and BA1 which correspond 15 to the most significant bit(MSB) of row address becomes 0.

When only the address A0 is 0, a self-refresh operation is performed on a quarter cell array of a bank by selecting a "QUARTER OF BANK". Here, both of the bank address bits BA0 and BA1, which are the two most 20 significant bits of the row address, become 0.

Additionally, the case when only the address bit A2 is 0, the case when the only the address bit A2 is 1, and the case when all address bits A0~A2 are 1 are reserved for future use(RFU).

Fig. 5 is a timing diagram illustrating a self-refresh entry and exit mode according to an embodiment of the present invention.

First, a PASR type is preset to the EMRS code. When 5 a self-refresh command SREFCMD is inputted, a self-refresh operation is performed according to the preset PASR type. As a result, a selective self-refresh operation is performed on cell arrays corresponding to the PASR type according to the EMRS code.

10 Next, when a clock enable signal CKE is enabled to a high level and a self-refresh exit command SREX is inputted, a self-refresh operation is finished and a normal operation is performed. In the normal mode, a self-refresh operation is performed on all cell arrays.

15 Thereafter, when the self-refresh command SREFCMD is re-inputted, the PASR operation is performed according to the preset EMRS code.

Fig. 6 is a structural diagram illustrating a self-refresh apparatus according to an embodiment of the present 20 invention.

The self-refresh apparatus of Fig. 6 comprises an address buffer 10, a command decoder 20, a refresh counter 30, a PASR decoder 40, a refresh controller 50, RAS (Row Address Strobe) generators 60, 70, 80 and 90, an internal

address counter 100, a row address pre-decoder 110, bank control blocks 120, 130, 140 and 150, and cell array banks 160, 170, 180 and 190.

Here, the address buffer 10 buffers an externally inputted address  $A<0:n>$ , and outputs the buffered address  $ADD<0:n>$ .

The command decoder 20 decodes an externally inputted command CMD, and outputs an auto-refresh signal AREF, a self-refresh signal SREF, a mode register set signal MREGSET and a normal operation signal N\_ACT.

When a self-refresh signal SREF representing a self-refresh operation is activated, the refresh counter 30 activates a refresh oscillator and makes it output a self-refresh requiring signal SREF\_REQ having a predetermined cycle.

Fig. 7 is a diagram illustrating the relationship between a self-refresh signal SREF and a self-refresh requiring signal SREF\_REQ when an external command is inputted.

The self-refresh signal SREF is activated in response to the self-refresh command SREFCMD, and inactivated in response to the self-refresh exit command SREX. In a self-refresh mode, the refresh counter 30 generates the self-refresh requiring signal SREF\_REQ as a pulse signal to have

a predetermined cycles. For example, when a memory device has a refresh rate for performing a refresh operation on a cell array of 8K for 64msec, the self-refresh requiring signal SREF\_REQ is generated per 7.8 $\mu$ sec.

5 The PASR decoder 40 decodes the mode register set signal MREGSET and the self-refresh signal SREF applied from the command decoder 20, and addresses add<n>, add<n-1> and add<0:2> from the address buffer 10 to generate control signals for performing a PASR operation depending on types 10 of PASR. When a PASR type is a "HALF OF BANK" or "QUARTER OF BANK" on a bank, the PASR decoder 40 outputs control signals RASR\_BH and PASR\_BQ for identifying corresponding PASR types, and control signals PASR\_BK1 and PASR\_BK23 for selectively activating other banks than the bank.

15 The refresh controller 50 receives the auto-refresh signal AREF and the self-refresh signal SREF from the command decoder 20, the self-refresh requiring signal SREF\_REQ from the refresh counter 30, the control signals PASR\_BH and PASR\_BQ from the PASR decoder 40, and internal 20 addresses I\_ADD<n-2> and I\_ADD<n-3> from the internal address counter 100, and generates an internal operation signal I\_ACT and a refresh operation signal R\_ACT for controlling a refresh operation. Here, the internal operation signal I\_ACT is to activate the internal address

counter 100 in a predetermined cycle in a refresh (auto-refresh or self-refresh) mode. The refresh operation signal R\_ACT is to control a refresh operation on cell arrays of a corresponding bank by controlling the RAS generators 60~90.

When the control signals PASR\_BH and PASR\_BQ are activated, the refresh controller 50 selectively activates the refresh operation signal R\_ACT according to the internal addresses I\_ADD<n-2> and I\_ADD<n-3> from the 10 internal address counter 100, but the refresh controller 50 continuously activates the internal operation signal I\_ACT

The RAS generator 60 receives a normal operation signal N\_ACT, a bank selecting address ADD\_BK0 and a refresh operation signal R\_ACT, and outputs a row active signal ROW\_ACT<0> into a bank control block 120 for activating a bank 160.

The RAS generator 70 receives a normal operation N\_ACT, a bank selecting address ADD\_BK1, a refresh operation signal R\_ACT and a control signal PASR\_BK1, and 20 outputs a row active signal ROW\_ACT into a bank control block 130 for activating a bank 170.

The RAS generator 80 receives a normal operation signal N\_ACT, a bank selecting address ADD\_BK2, a refresh operation signal R\_ACT and a control signal PASR\_BK23, and

outputs a row active signal ROW\_ACT into a bank control block 140 for activating a bank 180.

The RAS generator 90 receives a normal operation signal N\_ACT, a bank selecting address ADD\_BK3, a refresh operation signal R\_ACT and a control signal PASR\_BK23, and outputs a row active signal ROW\_ACT into a bank control block 150 for activating a bank 190.

The internal address counter 100 counts internal addresses in a predetermined cycle corresponding to a refresh rate during the refresh operation in response to the internal operation signal I\_ACT from the refresh controller 50, and then outputs an internal address I\_ADD<0:n> into the row address pre-decoder 110. The internal address counter 100 outputs internal addresses I\_ADD<n-2> and I\_ADD<n-3> into the refresh controller 50. According to the internal addresses I\_ADD<n-2> and I\_ADD<n-3>, the refresh controller 50 may identify whether the refresh operation is performed on a half or quarter of bank.

The row address pre-decoder 110 pre-decodes an externally inputted address ADD<0:n-2> and the internal address I\_ADD from the internal address counter 100, and outputs the pre-decoded addresses into each bank control block 120~150.

In a normal mode, the row address pre-decoder 110

generates a row address  $\text{ROW\_ADD}_{0:n-2}$  by decoding the external address  $\text{ADD}_{0:n-2}$ , and outputs the row address  $\text{ROW\_ADD}_{0:n-2}$  into each bank control block 120~150. In a refresh mode, the row address pre-decoder 110 generates the 5 row address  $\text{ROW\_ADD}_{0:n-2}$  by decoding the internal address  $\text{I\_ADD}_{0:n-2}$ , and outputs the row address  $\text{ROW\_ADD}_{0:n-2}$  into each bank control block 120~150.

Each bank control block 120~150 controls each bank 160~190 comprising cell arrays.

10 Here, the address  $\text{ADD}_{0:n}$  is a row address ranging from 0 to n corresponding to the memory depth, and the most significant bit of row address is used as a bank selecting address for selecting a bank.

15 Since two bank selecting addresses are required in a memory having a four-bank structure, the addresses  $\text{ADD}_{n}$  and  $\text{ADD}_{n-1}$  are used as bank selecting addresses. And the address  $\text{ADD}_{0:n-2}$  is used for selecting cell arrays and wordlines of each selected bank.

20 Fig. 8 is a detailed structural diagram illustrating the PASR decoder 40 of Fig. 6.

The PASR decoder 40 comprises an EMRS decoder 41, address latches 42~44, and a PASR controller 45. The EMRS decoder 41 decodes a EMRS command. The address latches 42~44 latch addresses  $\text{ADD}_{0}$ ,  $\text{ADD}_{1}$  and  $\text{ADD}_{2}$

representing PASR codes when an EMRS command inputted. The PASR controller 45 outputs a control signal for performing a PASR operation depending on PASR types.

The EMRS decoder 41 decodes the mode register set signal MREGSET and the bank selecting addresses ADD<n> and ADD<n-1>, and outputs a register set control signal EMRSP.

The address latches 42~44 latch addresses ADD<0>, ADD<1> and ADD<2> in response to the mode register set signal MREGSET, the register set control signal EMRSP and the self-refresh signal SREF, and outputs register set addresses EMRSA<0>, EMRSA<1> and EMRSA<2>.

The PASR controller 45 selectively outputs control signals PASR\_BK1, PASR\_BK23, PASR\_BH and PASR\_BQ in response to the register set addresses EMRSA<0>, EMRSA<1> and EMRSA<2>. Here, the control signals PASR\_BK1 and PASR\_BK23 are to selectively activate banks in a PASR mode. The control signals PASR\_BH and PASR\_BQ are activated when PASR type is "HALF OF BANK" or "QUARTER OF BANK" respectively.

Fig. 9 is a detailed circuit diagram illustrating the EMRS decoder 41 of Fig. 8.

The EMRS decoder 41 comprises an inverter IV1 for inverting the bank selecting address ADD<n-1>, and a NAND gate ND1 for performing a NAND operation on an output

signal from the inverter IV1 and the bank selecting address ADD<n>. The EMRS decoder 41 comprises an inverter IV2 for inverting an output signal from the NAND gate ND1, and a NAND gate ND2 for performing a NAND operation on an output 5 signal from the inverter IV2 and the mode register set signal MREGSET and for outputting a register set control signal EMRSP.

The operation of the EMRS decoder 41 is described.

If the mode register set signal MREGSET is activated 10 in the command decoder 20 according to the externally applied EMRS command, the EMRS decoder 41 activates the register set control signal EMRSP corresponding to the EMRS code of Fig. 4 according to the states of bank selecting addresses ADD<n>=BA1 and ADD<n-1>=BA0 of the buffered 15 address ADD<0:n>.

Fig. 10 is a detailed circuit diagram illustrating the EMRS address latch of Fig. 8.

Each address latch 42~44 comprises a switch S/W<0> for selectively outputting address ADD<i> (here, i=0, 1, 2) 20 in response to the mode register set signal MREGSET, and a latch R1 for latching an output signal from the switch S/W<0>. Here, the latch R1 comprises inverters IV3 and IV4 wherein an output signal from the inverter IV3 is inputted into the inverter IV4 and an output signal from the

inverter IV4 is inputted into the inverter IV3.

Each address latch 42~44 also comprises a switch S/W<1> for selectively outputting an output signal from the latch R1 in response to the register set control signal

5 EMRSP, and a latch R2 for latching an output signal from the switch S/W<1>. Here, the latch R2 comprises inverters IV5 and IV6 wherein an output signal from the inverter IV5 is inputted into the inverter IV6 and an output signal from the inverter IV6 is inputted into the inverter IV5.

10 Each address latch 42~44 also comprises a NAND gate ND3 for performing a NAND operation on the self-refresh signal SREF and an output signal from the latch R2, and an inverter IV7 for inverting an output signal from the NAND gate ND3 and outputting the register set address EMRSA<i>

15 (here, i=0, 1, 2).

Each address latch 42~44 controls the switches S/W<0> and S/W<1> in response to the mode register set signal MREGSET and the register set control signal EMRSP, and latches the address ADD<0:2> inputted with the EMRS command.

20 Each address latch 42~44 also activates the register set address EMRSA<i> depending on input of the self-refresh signal SREF. Although the address latch latches the EMRS codes, the register set address EMRSA<i> is not activated when the self-refresh signal SREF is inactivated.

Fig. 11 is a detailed circuit diagram illustrating the PASR controller 45 of Fig. 8.

An inverter IV8 inverts the register set address EMRSA<0>, and outputs a register set address EMRSAZ<0>. An 5 inverter IV9 inverts the register set address EMRSA<1>, and outputs a register set address EMRSAZ<1>. An inverter IV10 inverts the register set address EMRSA<2>, and outputs a register set address EMRSAZ<2>.

A NAND gate ND4 performs a NAND operation on the 10 register set address EMRSAZ<0> and the register set address EMRSA<1>. A NAND gate ND5 performs a NAND operation on an output signal from the NAND gate ND4 and the register set address EMRSAZ<2>. An inverter IV11 inverts an output signal from the NAND gate ND5, and outputs the control 15 signal PASR\_BK1.

A NAND gate ND6 performs a NAND operation on the register set address EMRSA<0> and the register set address EMRSAZ<1>. A NAND gate ND7 performs a NAND operation on the register set address EMRSAZ<2> and an output signal 20 from the NAND gate ND6.

A NOR gate NOR1 performs a NOR operation on output signals from the NAND gates ND5 and ND7 to output a control signal PASR\_BK23.

A NAND gate ND8 performs a NAND operation on the

register set addresses EMRSA<0>, EMRSAZ<1> and EMRSA<2>. A NAND gate ND9 performs a NAND operation on the register set addresses EMRSAZ<0>, EMRSA<1> and EMRSA<2>. An inverter IV12 inverts an output signal from the NAND gate ND8 to 5 output a control signal PASR\_BH. An inverter IV13 inverts an output signal from the NAND gate ND9 to output a control signal PASR\_BQ.

The operation of the PASR controller 45 is described.

Since the self-refresh signal SREF is inactivated in 10 a normal mode, the register set address EMRSA<0:2> becomes at a low level (see Fig. 10). As a result, the control signals PASR\_BK1 and PASR\_BK23 become at a high level, and the control signals PASR\_BH and PASR\_BQ become at a low level.

15 In a self-refresh mode, the register set address EMRSA<0:2> represents the level of the address ADD<0:2> inputted with the EMRS command. When the EMRS command is inputted, the level of the control signals change depending on the states of each address ADD<0>, ADD<1> and ADD<2> 20 like the following.

As shown in Fig. 4, if the EMRS code is "ALL BANKS", the control signals PASR\_BK1 and PASR\_BK23 become at the high level, and the control signals PASR\_BH and PASR\_BQ become the low level.

If the EMRS code is a "HALF ARRAY", the control signal PASR\_BK1 becomes at the high level, and the control signals PASR\_BK23, PASR\_BH and PASR\_BQ become at the low level.

5 If the EMRS code is a "QUARTER ARRAY", the control signals PASR\_BK1, PASR\_BK23, PASR\_BH and PASR\_BQ become at the low level.

If the EMRS code is a "HALF OF BANK", the control signal PASR\_BH becomes at the high level, and the control signals PASR\_BK1, PASR\_BK23 and PASR\_BQ become at the low level.

10 If the EMRS code is a "QUARTER OF BANK", the control signal PASR\_BQ becomes at the high level, and the control signals PASR\_BK1, PASR\_BK23 and PASR\_BH become at the low level.

15 The PASR controller 45 selectively outputs the control signals PASR\_BH and PASR\_BQ for identifying the PASR types on a bank, and the control signals PASR\_BK1 and PASR\_BK23 for selectively activating the RAS generators 20 70~90 depending on the preset EMRS codes of Fig. 4.

Fig. 12 is a detailed circuit diagram illustrating the refresh controller 50 of Fig. 6.

A NAND gate ND10 performs a NAND operation on the internal address  $I\_ADD< n-2 >$  and the control signal PASR\_BH.

A NOR gate NOR2 performs a NOR operation on the internal addresses  $I\_ADD< n-2 >$  and  $I\_ADD< n-3 >$ . An inverter IV14 inverts an output signal from the NOR gate NOR2. A NAND gate ND11 performs a NAND operation on an output signal 5 from the inverter IV14 and the control signal PASR\_BQ. A NAND gate ND12 performs a NAND operation on output signals from the NAND gates ND10 and ND11. An inverter IV15 inverts an output signal from the NAND gate ND12.

An NAND gate ND13 performs a NAND operation on the 10 self-refresh signal SREF and the self-refresh request signal SREF-REQ. An inverter IV16 inverts an output signal from the NAND gate ND13. A NOR gate NOR3 performs a NOR operation on the auto-refresh signal AREF and an output signal from the inverter IV16. An inverter IV17 inverts an 15 output signal from the NOR gate NOR3 to output the internal operation signal I\_ACT.

A NAND gate ND14 performs a NAND operation on output signals from the inverters IV15 and IV17. An inverter IV18 inverts an output signal from the NAND gate ND14 to output 20 the refresh operation signal R\_ACT.

Fig. 13 is a detailed circuit diagram illustrating the RAS generator 60 of Fig. 6.

The RAS generator 60 comprises PMOS transistors P1 and P2, and NMOS transistors N1 and N2 connected in series

between power voltage VDD and ground GND. Here, a gate of the PMOS transistor P1 receives a normal operation signal N\_ACT, and a gate of the PMOS transistor P2 receives a refresh operation signal R\_ACT.

5 A gate of the NMOS transistor N1 receives the normal operation signal N\_ACT, and a gate of the NMOS transistor N2 receives the bank selecting address ADD\_BK<0>.

NMOS transistors N3 and N4 connected in series between a command drain of the PMOS transistor P2 and the 10 NMOS transistor N1 and a ground GND. Here, a gate of the NMOS transistor N3 receives the refresh operation signal R\_ACT, and a gate of the NMOS transistor N4 receives a power voltage VDD.

An inverter IV18 inverts an output signal from a 15 common drain of the NMOS transistors N1 and N3, and outputs a row active signal ROW\_ACT<0> for activating the bank 160.

Fig. 14 is a detailed circuit diagram illustrating the RAS generators 70~90 of Fig. 6.

The configuration of the RAS generators 70~90 is the 20 same as that of the RAS generator 60 of Fig. 13 except that a gate of the NMOS transistor N4 receives the control signal PASR\_BK<j>(j=1, 23).

In the RAS generator 60 unlike the RAS generators 70~90, the bank 160 is always selected regardless of the

PASR types in a refresh mode because the gate of the NMOS transistor N4 connected to a power voltage VDD does not receive a control signal from the PASR decoder 40.

If a command CMD representing the EMRS is externally inputted, the command decoder 20 activates the mode register set signal MREGSET.

The PASR decoder 40 decodes the mode register set signal MREGSET and the addresses ADD<0:2>, ADD<n> and ADD<n-1> buffered in the address buffer 10, and outputs a control signal depending on the EMRS codes. The latched information in the PASR decoder 40 is maintained at a latched state before other EMRS code are inputted.

In a normal mode, the PASR decoder 40 activates the control signals PASR\_BK1 and PASR\_BK23 so that the RAS generators 70~90 may be activated.

If one of the RAS generators 60~90 is activated depending on the states of the bank selecting addresses ADD<n> and ADD<n-1>, one of the banks 160~190 is activated in response to the row active signal ROW\_ACT. The row address pre-decoder 110 generates the row address ROW\_ADD<0:n-2> by decoding the external address ADD<0:n-2> of the corresponding bank, thereby activating corresponding wordlines of a selected bank.

If the self-refresh command SREFCMD is externally

inputted, the self-refresh signal SREF representing a self-refresh state is activated by the command decoder 20. If the self-refresh signal SREF is activated, the PASR decoder 40 decodes the latched PASR information to output the 5 control signals PASR\_BK1 and PASR\_BK23, PASR\_BH and PASR\_BQ into the RAS generators 70~90 and the refresh controller 50, respectively.

As the self-refresh signal SREF is activated, the refresh counter 30 operates a refresh oscillator to 10 generate a self-refresh requiring signal SREF\_REQ in a predetermined cycle and output the signal into the refresh controller 50.

As the self-refresh signal SREF is activated, the refresh controller 50 generates the internal operation 15 signal I\_ACT in response to the self-refresh requiring signal SREF\_REQ and generates the refresh operation signal R\_ACT in response to the control signals PASR\_BH and PASR\_QH and the internal addresses I\_ADD<n-2> and I\_ADD<n-3>.

20 When the EMRS code is "ALL BANKS" in a self-refresh mode, the control signals PASR\_BK1 and PASR\_BK23 of the PASR decoder 40 are outputted at the high level. As a result, the RAS generators 60~90 are maintained at an active state. The row address pre-decoder 110 receives the

internal address  $I\_ADD<0:n-2>$  from the internal address counter 100, and outputs the address as the row address  $ROW\_ADD<0:n-2>$  so that corresponding wordlines may be activated in all banks 160~190.

5 When the EMRS code is a "HALF ARRAY" in a self-refresh mode, the PASR decoder 40 activates the control signal  $PASR\_BK1$  but inactivates the control signal  $PASR\_BK23$ . As a result, only the RAS generators 60 and 70 are activated. The row address pre-decoder 110 receives the 10 internal address  $I\_ADD<0:n-2>$  from the internal address counter 100, and outputs the address as the row address  $ROW\_ADD<0:n-2>$  to activate corresponding wordlines in the banks 160 and 170. Since the RAS generators 80 and 90 are inactivated in response to the control signal  $PASR\_BK23$ , 15 the banks 180 and 190 do not operate.

When the EMRS code is a "QUARTER ARRAY" in a self-refresh mode, the PASR decoder 40 inactivates the control signals  $PASR\_BK1$  and  $PASR\_BK23$ . As a result, only the RAS generator 60 is maintained at an active state. The row 20 address pre-decoder 110 receives the internal address  $I\_ADD<0:n-2>$  from the internal address counter 100, and outputs the address as the row address  $ROW\_ADD<0:n-2>$ , thereby activating corresponding wordlines in the bank 160. Since the RAS generators 70~90 are inactivated in response

to the control signals PASR\_BK1 and PASR\_BK23, the banks 170~190 do not operate.

Fig. 15 is a timing diagram illustrating the operation of control signals for controlling the RAS 5 generator.

Fig. 15 shows the states of the refresh operation signal R\_ACT and the internal operation signal I\_ACT depending on phase change of the internal address I\_ADD<n-2> when the EMRS code is a "HALF OF BANK" during the PASR 10 operation.

As described above, if the active command ACT is inputted in a normal mode, the normal operation signal N\_ACT is activated, and the control signals PASR\_BK1 and PASR\_BK23 are also activated. As a result, the RAS 15 generators 60~90 become at an active state.

Next, if the auto-refresh command AREFCMD is externally inputted, the command decoder 20 outputs the auto-refresh signal AREF into the refresh controller 50. The refresh controller 50 which receives the auto-refresh 20 signal AREF activates the refresh operation signal R\_ACT and the internal operation signal I\_ACT, and outputs the signals into the RAS generators 60~90 and the internal address counter 100.

Here, the control signal PASR\_BH is at the low level

on a "HALF OF BANK", and the refresh operation signal R\_ACT is not controlled. The internal address counter 100 performs a count operation by activation of the internal operation signal I\_ACT. As a result, the internal address 5 I\_ADD<n-2> toggles after the preset time, and transits to a low level.

If the self-refresh command SREFCMD is inputted when the EMRS code is a "HALF OF BANK", the control signal PASR\_BH of the PASR decoder 40 is activated, and the 10 control signals PASR\_BQ, PASR\_BK1 and PASR\_BK23 are inactivated since the EMRS codes are A2=1, A1=0 and A0=1 in Fig. 4. As a result, the RAS generators 70~90 are inactivated, and the banks 170~190 do not operate.

The row address pre-decoder 110 generates the row 15 address ROW\_ADD<0:n-2> by decoding the internal address I\_ADD<0:n-2> counted in the internal address counter 100 so that corresponding wordlines may be activated in the bank 160. If the wordlines are consecutively activated and the self-refresh operation is completed on a half of the bank 20 160, the internal address I\_ADD<n-2> generated on the internal address counter 100 becomes at a high level on the rest half of the bank 160.

In the interval 16 where the internal address I\_ADD<n-2> becomes at the high level, the refresh

controller 50 prevents the self-refresh requiring signal SREF\_REQ from being transmitted into the refresh operation signal R\_ACT. As a result, the refresh operation signal R\_ACT is inactivated. If the refresh operation signal R\_ACT is inactivated, the RAS generator 60 is also inactivated, and the bank 160 does not operate. As a result, the self-refresh operation is performed on a half of the bank 160.

However, since the internal operation signal I\_ACT generated from the refresh controller 50 is not controlled by the control signal PASR\_BH as shown in Fig. 12, the internal operation signal I\_ACT is generated in response to the self-refresh requiring signal SREF\_REQ regardless of the PASR types. As a result, the internal address counter 100 performs a count operation on all addresses during a predetermined refresh rate although the self-refresh operation is not performed on the rest half of the bank 160.

The refresh operation signal R\_ACT for activating the RAS generators 60~90 is generated until a predetermined internal address is counted. The internal operation signal I\_ACT is generated on the whole bank 160 in response to the self-refresh request signal SREF\_REQ. Although the refresh operation is performed on cell arrays corresponding to the half of the bank 160 ("HALF OF BANK") during the

predetermined refresh rate, the whole cell arrays of the bank 160 are counted. As a result, the refresh operation starts from the first wordline 11 of the bank 160 although the auto-refresh operation is performed after completion of 5 the corresponding PASR operation. That is, each wordline is refreshed per refresh rate of 64msec.

When the EMRS code is a "QUARTER OF BANK" in a self-refresh operation, the PASR codes are A2=1, A1=1 and A0=0. As a result, the control signal PASR\_BQ of the PASR decoder 10 40 is activated, and the control signals PASR\_BH, PASR\_BK1 and PASR\_BK23 are maintained at the inactivated state. Then, the RAS generators 70~90 are inactivated, and the banks 170~190 do not operate.

The row address pre-decoder 110 generates the row 15 address ROW\_ADD<0:n-2> by decoding the internal address I\_ADD<0:n-2> counted in the internal address counter 100, thereby activating wordlines in the bank 160. If the wordlines are consecutively activated, and the self-refresh operation is completed on the quarter of the bank 160, the 20 internal address I\_ADD<n-3> generated from the internal address counter 100 becomes at the high level on the next quarter of the bank 160.

In an interval where the internal address I\_ADD<n-3> becomes at the high level, the refresh controller 50

prevents the self-refresh request signal 'SREF\_REQ' from being transmitted into the refresh operation signal R\_ACT. As a result the refresh operation signal R\_ACT is inactivated.

5        In an interval corresponding to the rest half of the bank 160, the internal address I\_ADD<n-3> becomes at the low level again. However, since the internal address I\_ADD<n-2> becomes at the high level like the above-described "HALF OF BANK", the refresh operation signal  
10      R\_ACT is continuously maintained at the inactivated state.

      If at least one of two most significance bites (MSBs) in the bank 160 becomes at a high level, the refresh operation signal R\_ACT is inactivated. However, since the internal operation signal I\_ACT is not controlled by the  
15      internal addresses I\_ADD<n-2> and I\_ADD<n-3> and control signals PASR\_BH and PASR\_BQ, the internal operation signal I\_ACT is generated in response to the self-refresh requiring signal SREF\_REQ regardless of the PASR types.

      Although the self-refresh operation is not performed  
20      on the rest three quarters of the bank 160, all addresses of the bank 160 are counted during the predetermined refresh rate.

      As discussed earlier, when a partial array self-refresh (half of bank or quarter of bank) operation is

performed, a self-refresh operation is performed until a predetermined internal address is counted depending on PASR types. However, counting for the internal address is performed for the whole internal address. As a result, the  
5 error of refresh rate can be prevented.